

School of

Electronics and Communication Engineering

**ADLD**

Course Project On

**“Digital Clock on FPGA”**

Team No: 15

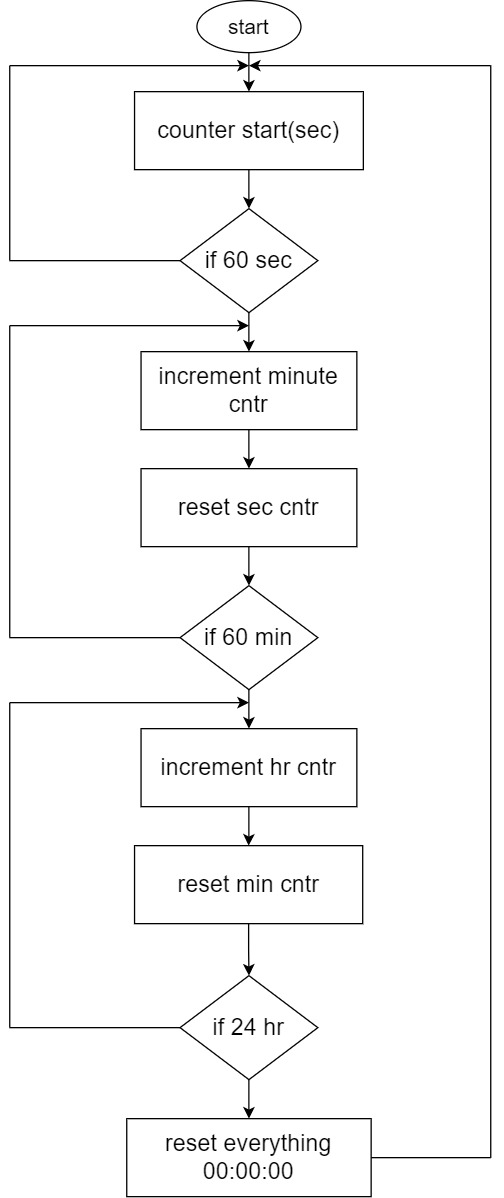
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Semester: VI (2022)

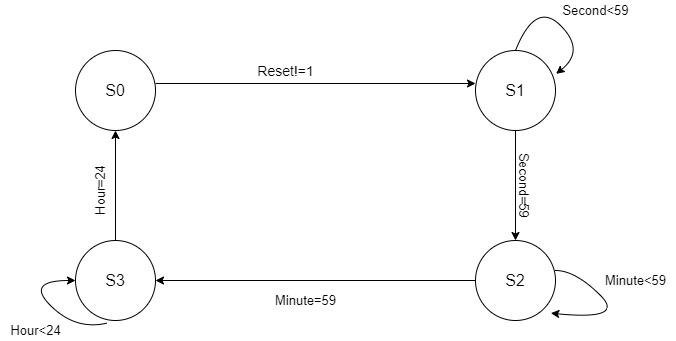
**Problem Statement:**

Digital Clock on FPGA

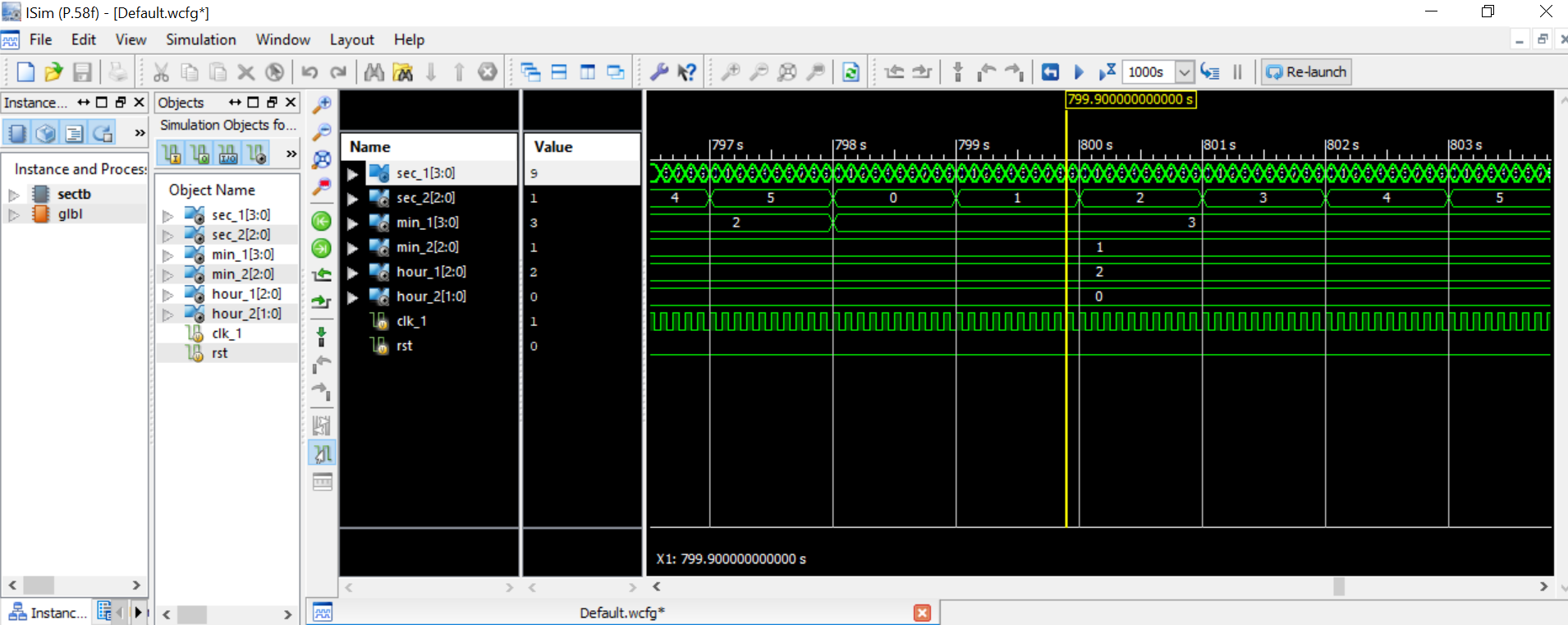
**Flow Chart:**

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**FSM:**

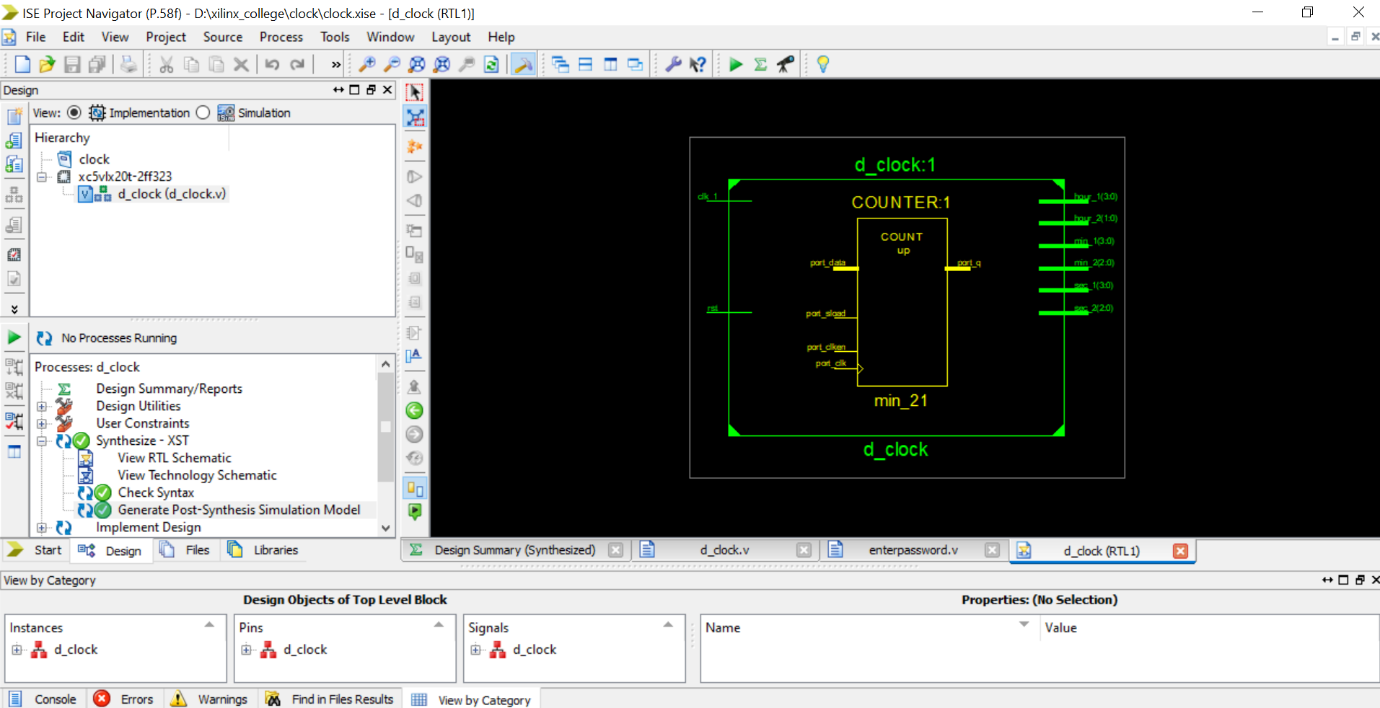


**Simulation Results:**



**Synthesis:**

RTL schematic:



Technological schematic:

